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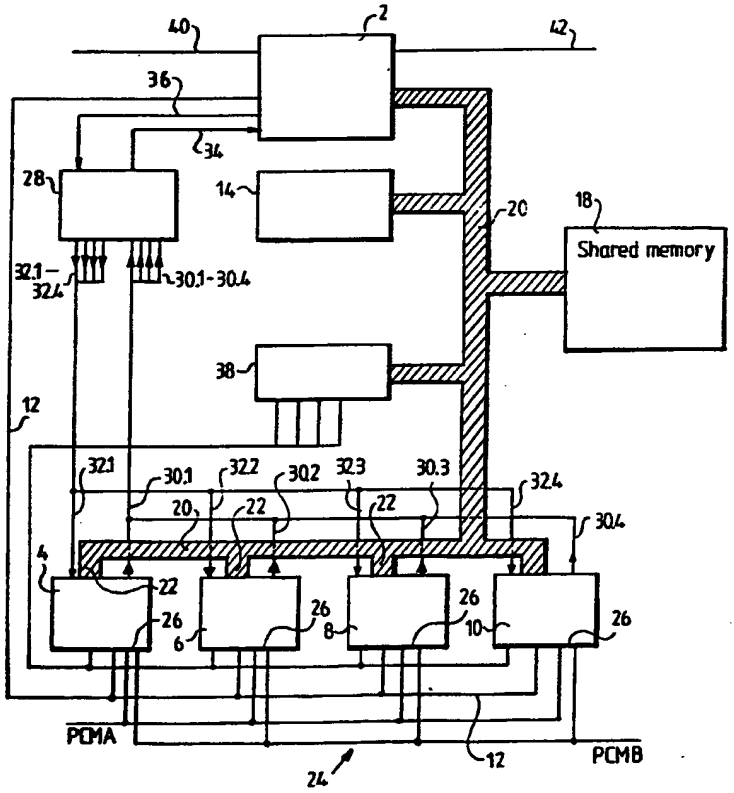
(54) Title: SIGNAL HANDLING SYSTEM WITH A SHARED DATA MEMORY

(57) Abstract

A signal processing system includes a superior control processor (2) and a number of digital signal processors (4-10), which are controlled by the control processor and normally operate internally with real time applications. A shared data memory (18) is included with a bus (20), on which the control processor normally is bus master, and to which the signal processors have access. An arbitration logic (28) controls the access of the processors (4-10) to the shared data memory. The signal processors (4-10) are directly connected to the bus (20) and normally keep their data and address buses (22) on a high impedance level with respect thereto.



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Signal handling system with a shared data memory.

Technical field of the invention.

The present invention relates to a signal processing system, including

a superior control processor,

a number of digital signal processors, which are controlled by the control processor and normally operate internally with real time applications,

a shared data memory with a bus, on which the control processor normally is bus master, and to which the signal processors have access, and

an arbitration logic, which controls the access of the processors to the shared data memory.

Description of related art.

Common to known earlier circuits of the kind defined by way of introduction is that they require external buffers between each signal processor and the bus.

Through SE-B-442,352 a data processing system of essentially the kind indicated by way of introduction is known. The system includes a central computer, a bus, a memory, a plurality of peripheral computers, and an arbitration logic controlling the access of the computers to the memory. As appears from page 2, from line 14, in this document, has normally, however, in this system only the central computer access to the memory via the bus, whereas the peripheral computers are disconnected from the bus line.

Through GB-A-1,600,756 a processor system is known including a superior control processor and a number of subordinate processors. An arbitration circuit controls all access to a common memory from buses connecting together the subordinate processors and includes address lines and data lines. A bus assigning function in the arbitration circuit provides sequencial bus access for the subordinate processors. A bus access logic in each such processor controls request for access to the bus.

US-A-5,067,071 describes and shows a multiprocessor system with a memory shared by all processor modules. A bus arbitration function is arranged in a system control module for

controlling the access of the processors to the common memory. The data buses and address buses of the processor modules are connected via tranceivers to the common system bus. The system handles request and access.

ES-A-4,499,538 relates to access arbitration for a system with several processors and a common bus. A common resource consists of a number of memories. A plurality of processors can via a bus obtain access to the common resource. Each one of the processors has assigned thereto an own arbitration function.

In EP-A1-464,708 there is described a bus system with a number of processors and a common memory. A central circuit includes arbitration logic for handling access of the processors to the common memory.

US-A-4,803,617 describes a multiprocessor system with a common mass memory. Each processor emits a request when it needs access to a position in the main memory via the bus. During the time data transaction is performed all other processors must wait for the bus being free. An arbitrator arranges access of the processors to the bus.

From US-A-4,924,380 a similar system as that just described is known. Beyond this, technique is described for providing a better bus effectivity by means of an arbitration system consisting of two rotating queues with a fixed priority between the queues.

Summary of the invention.

The object of the present invention is to minimize, in a signal processing system of the kind defined by way of introduction, the number of necessary components, and suggest a solution where access to the shared memory can be attained with short delay and without master-slave configuration and external buffers.

This object has been attained in that, in accordance with the invention, the signal processors are directly connected to the bus and normally keep their data and adress buses on a high impedance level with respect thereto.

Brief description of the drawing.

The invention will now be described more closely with reference to a schematic block diagram of a signal handling system shown on the attached drawing.

Preferred embodiment.

The system shown in Fig. 1 includes five microprocessors, viz. one superior control processor 2 and four digital signal processors 4, 6, 8 and 10. The processors 2-10 have a common link 12, having as a first function to serve as a signalling channel, via which the control processor 2 performs operation and maintainance functions as well as certain real time operations. The digital signal processors 4, 6, 8 and 10 perform real time operations and execute programs internally.

The control processor 2 has an external program memory in the form of a PROM 14. This PROM 14 also includes application programs for the digital signal processors 4, 6, 8 and 10. The link 12 also serves for transferring the application program from the processor 2 to the digital signal processors, one at a time.

A RAM 18 is a shared memory between the control processor 2 and the signal processors 4-10. To this RAM 18 a bus 20, indicated with dashed lines, leads, that includes data buses and address buses as well as read strobes and write strobes. The control processor 2 is normally bus master for the bus 20 and the signal processors are directly connected to the bus 20 by means of their own buses 22.

The signal processors 4, 6, 8 and 10 have an inner RAM (not shown) for programs and data, as well as an inner ROM (not shown) for start up programs. This implies that each signal processor can operate internally with its own application program. This application program contains instructions for keeping the bus 22 of the corresponding signal processor on a high impedance level. No external data access occurs except when the signal processor desires to use the shared memory 18.

Data from/to a PCM channel 24 with an input PCMA and an output PCMB are clocked in/out via serial ports 26 of the signal processors.

As mentioned the signal processors 4-10 keep their buses 22
on a high impedance level and are directly connected to the bus 20 without mediation by any external buffer. The four signal processors are designed to send, in case of desired access to the memory 18, an inquiry signal to an arbitration logic 28 for the bus 20 via each an inquiry line 30.1, 30.2, 30.3 and 30.4, respectively, and to receive a confirmation, if any, on the

request from the arbitration logic via each a confirmation line 32.1, 32.2, 32.3 and 32.4, respectively.

One purpose of the arbitration logic 28 is to send, at receipt of a demand for bus access in the form of such an inquiry signal from any of the signal processors, a corresponding demand to the control processor via a line 34. If the bus 20 is available the control processor replies via a line 36 to the arbitration logic 28 with a signal implying that the demand has been accepted. The arbitration logic then informs this to the inquiring signal processor via the confirmation line of the latter. Thereby the ownership to the bus 20 is transferred to the signal processor in question.

If the bus 20 is requested by any signal processor when it is owned by the control processor 2 and not available, i.e. the latter uses the bus, the arbitration logic 28 will let the request wait until the bus becomes free. If more signal processors simultaneously have requested the bus it is assigned by rotating assignment.

The block diagram on the drawing also includes a time slot assignment logic 38 controlled from the control processor 2 and distributing the time slots of the PCM channels to the different signal processors 4-10. The distribution is completely free which implies that a time slot can be taken care of by any of the four signal processors. The logic 38 generates synchronization pulses, one for each time slot, both for the sending and for the receiving direction. The pulses are generated to all signal processors working in the configuration in question. If no time slot is active no pulses are generated by the logic 38.

At 40 and 42 input and output signalling channels to the control processor are indicated.

Certain details and functions in the system shown and described have not been described in more detail above. In such cases it has been presumed that it is the question either of matter, about which the man of the art does not need any closer information for being able to practice the invention, or matter not having any relationship with the invention.

Claims.

1. A signal processing system, including

a superior control processor (2),

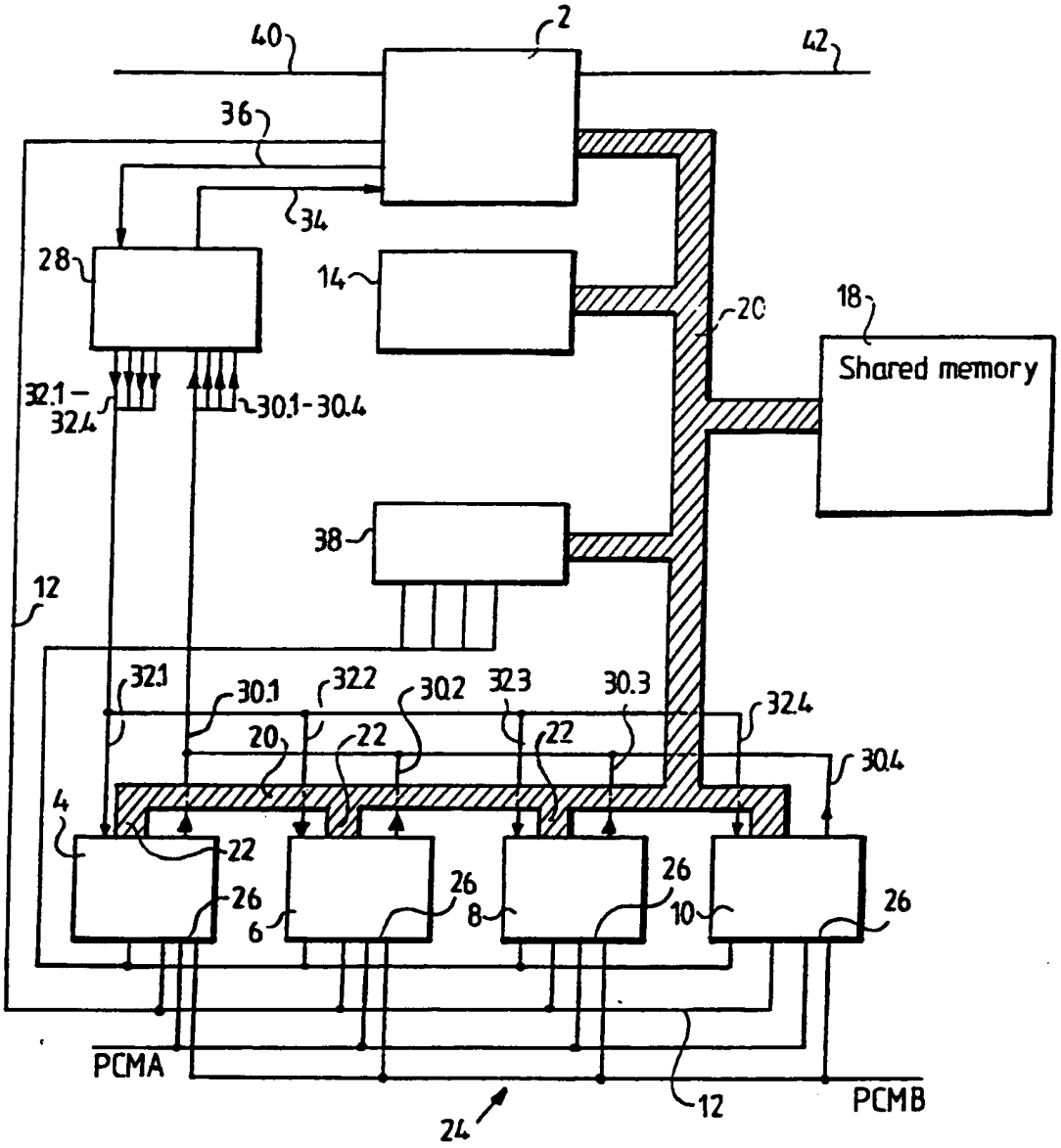
a number of digital signal processors (4-10), which are controlled by the control processor and normally operate internally with real time applications,

a shared data memory (18) with a bus (20), on which the control processor normally is bus master, and to which the signal processors have access, and

an arbitration logic (28), which controls the access of the processors (4-10) to the shared data memory,

characterized in that

the signal processors (4-10) are directly connected to the bus (20) and normally keep their data and address buses (22) on a high impedance level with respect thereto.


40
2
42
36
34
28
14
20
18
Shared memory
32.1 - 32.4
30.1 - 30.4
38
12
32.1
30.1
32.2
30.2
32.3
30.3
32.4
20
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PCMA
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PCMB
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 93/00840

A. CLASSIFICATION OF SUBJECT MATTER

IPC5: G06F 13/366
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC5: G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 4611275 (JEAN-FRANCOIS GARNIER), 9 Sept 1986 (09.09.86), column 1, line 67 - column 2, line 54, figure 1 —	1
A	US, A, 4504906 (HIROSHI ITAYA ET AL), 12 March 1985 (12.03.85), column 4, line 1 - line 54, figure 4 —	1
A	US, A, 4523274 (YASUSHI FUKUNAGA ET AL), 11 June 1985 (11.06.85), column 2, line 63 - line 68, figure 2 —	1

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
17 January 1994	24 -01- 1994
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 93/00840

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 5067071 (DAVID J. SCHANIN ET AL), 19 November 1991 (19.11.91), figure 1, abstract -- --------	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

27/11/93

International application No.
PCT/SE 93/00840

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